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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	10/666,742	
	Filing Date	September 19, 2003	
	First Named Inventor	Wood et al.	
	Art Unit	2812	
	Examiner Name	A. Ghyka	
Total Number of Pages in This Submission	18	Attorney Docket Number	2269-6095US (03-0593.00/US)

**ENCLOSURES (check all that apply)**

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment / Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Reply to Missing Parts/ Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input checked="" type="checkbox"/> Appeal Brief (12 pages) with Claims Appendix (4 pages) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input type="checkbox"/> Other Enclosure(s) (please identify below):
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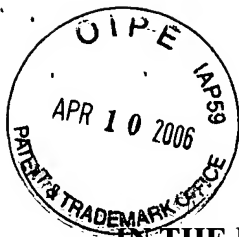
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**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

**In re Application of:** Wood et al.

**Serial No.:** 10/666,742

**Filed:** September 19, 2003

**For:** METHODS FOR THINNING  
SEMICONDUCTOR SUBSTRATES THAT  
EMPLOY SUPPORT STRUCTURES  
FORMED ON THE SUBSTRATES  
(Amended)

**Confirmation No.:** 6057

**Examiner:** A. Ghyka

**Group Art Unit:** 2812

**Attorney Docket No.:** 2269-6095US  
(03-0593.00/US)

**NOTICE OF EXPRESS MAILING**

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**APPEAL BRIEF**

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Attn: Board of Patent Appeals and Interferences

Sirs:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R.

§ 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

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I. REAL PARTY IN INTEREST

U.S. Application Serial No. 10/666,742 (hereinafter “the ‘742 Application”), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter “the Office”) at Reel No. 015025, Frame No. 0337. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

II. RELATED APPEALS AND INTERFERENCES

Neither Appellants nor their attorneys of record are aware of any appeals, interferences, or other proceedings that would affect the Board’s decision in the above-referenced appeal.

III. STATUS OF CLAIMS

The ‘742 Application was filed with sixty-nine (69) claims on September 19, 2003.

Claims 1-16 and 35-69 were withdrawn from consideration following restriction and species election requirements.

Claims 1-16 and 35-69 have been canceled without prejudice or disclaimer. Claims 17-34 remain pending in the above-referenced application.

Final rejections were presented against each of claims 17-34.

IV. STATUS OF AMENDMENTS

The ‘742 Application was filed on September 19, 2003, with sixty-nine (69) claims.

The Examiner issued restriction and species election requirements in an action dated February 14, 2005. A preliminary amendment and response to the restriction requirement was mailed on February 28, 2005, and received a filing date of March 4, 2005. Claims 1-16 and 35-69 were canceled without prejudice or disclaimer. A non-substantive preliminary amendment was made to claim 21 of the elected claims.

On May 23, 2005, a first action on the merits was mailed. That action indicated that claims 17-34 had been considered and stood rejected. In response, an amendment was mailed on August 23, 2005, and received a filing date of August 31, 2005. In that Amendment, claims 18 and 29 were amended. In addition, explanations as to the patentability of claims 17-34 were provided.

On November 15, 2005, a second and final action on the merits was mailed. That action indicated that claims 17-34 had been reconsidered, but the initial rejection of May 23, 2005 was maintained. In a response mailed on January 16, 2006, which received a filing date of January 18, 2006, further explanations as to the patentability of claims 17-34 were provided.

The Examiner again rejected Appellant's reasoning, as evidenced by the comments that accompanied the Advisory Action dated January 30, 2006.

Despite careful explanations as to the patentability of the pending claims over the art upon which the Examiner's rejections have been based, the Examiner has continued to maintain rejections that were originally presented in the Office Action of May 23, 2005 (*see* Office Action of November 15, 2005 and Advisory Action of January 30, 2006).

In view of the Examiner's continued rejection of the claims, a Notice of Appeal was filed on February 8, 2006.

This APPEAL BRIEF, which is being filed on Monday, April 10, 2006, follows the Notice of Appeal and should be deemed to have been submitted within two months of the mailing date of the Notice of Appeal, as April 8, 2006, fell on a Saturday. 37 C.F.R. § 1.7.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The '742 Application includes claims that are directed to methods for thinning semiconductor substrates. Such a manufacturing method includes forming a support structure on an active surface of a substrate. Paragraph [0039]; FIGS. 2-4D. The substrate may comprise a full wafer bounded by an outer peripheral edge. Paragraph [0034]; FIG. 1. The support structure, which may be a support ring, may be substantially aligned with the outer peripheral edge or extends beyond the edge of the periphery. Paragraph [0040]; FIGS. 3, 4A, 4B. A consolidatable material, such as those used in stereolithographic or layered manufacturing techniques, may be used to form the support ring. Paragraph [0045]. These materials may comprise photoimagable polymers, thermoset polymers, photoresists, and the like. *Id.*

In an example of a method for forming a support structure, the semiconductor substrate may be submerged in fabrication tank that holds the unconsolidated material. Paragraph [0082]; FIG. 11A. Once positioned as desired, a focused consolidating energy, such as a laser, may be used to at least partially consolidate the unconsolidated material to form at least part of a first layer of the support structure. Paragraph [0083]; FIG. 11B. The substrate may be repositioned and a subsequent layer or layers formed by selectively exposing the unconsolidated material to the focused consolidated energy to at least partially consolidate the material. Paragraphs [0083] and [0084]; FIGS. 11B-11C.

The semiconductor substrate may be selectively thinned through various thinning processes known in the art, including, without limitation, back grinding, chemical etching, polishing, and the like. Paragraphs [0096]–[0098]; FIGS. 14A-14B. The material may be removed from the backside of the substrate. Paragraph [0098]; FIG. 14B. A thinned substrate that includes the support structure then may be transported for further processing.

Paragraphs [0100]–[0103]; FIGS. 15-16.

VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

(A) Whether, under 35 U.S.C. § 102(b), the subject matter recited in claims 17-20 is novel and, thus, patentable over the subject matter described in U.S. Patent 5,869,354 to Leedy, *et al.* (hereinafter “Leedy”);

(B) Whether, under 35 U.S.C. § 103(a), claims 21-34 are drawn to subject matter that is non-obvious and, thus, patentable over the subject matter taught in Leedy, in view of teachings from U.S. Patent 6,562,661 to Grigg, *et al.* (hereinafter “Grigg”).

VII. ARGUMENT

A. REJECTIONS UNDER 35 U.S.C. § 102

1. APPLICABLE LAW

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053

(Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

2. REFERENCE RELIED UPON

*Leedy*

The description of Leedy is limited to etching the back side 14 of a silicon substrate 10 to remove material from a central region thereof. A peripheral portion of the substrate 10 remains following the backside etch and serves as a frame 18. Col. 7, lines 35-68; Col. 8, lines 1-6; FIGS. 1a-1b.

Optionally, a preformed bonding frame or ring 19, typically a glass, quartz, or metal, may be bonded to the upper surface of the substrate 10, in which case the frame 18, which is a portion of the substrate 10, may be removed. Col. 9, lines 6-14; FIG. 1f.

3. ANALYSIS

Claims 17-20 have been rejected under 35 U.S.C. § 102(b) for reciting subject matter that is allegedly anticipated by the subject matter described in Leedy.

Independent claim 17 recites, among other things, a method for thinning a semiconductor substrate that includes “*forming* a support structure on an *active* surface of the semiconductor substrate.”

Contrary to the Examiner’s assertions set forth in the aforementioned office actions, Leedy does not expressly or inherently disclose each and every element of independent claim 17. As noted above, the disclosure of Leedy is limited to etching the backside of a substrate 10, with

a portion of the substrate 10 that remains on the backside serving as a frame 18. Col. 8, lines 1-6; Col. 9, lines 13-14 (“the original substrate 10 (which is backside etched) performs” the same function as optional bonding frame 19). Thus, the frame 18, which is on the backside of the substrate 10, is not “on the active surface of [a] semiconductor substrate,” as would be required for Leedy to expressly or inherently describe, or anticipate, each and every element of independent claim 17.

The optional *preformed* bonding frame 19 of Leedy, which is *bonded to* the substrate 10, is not *formed on* an active surface of a semiconductor substrate, as would be required for Leedy to expressly or inherently describe, or anticipate, each and every element of independent claim 17.

Because Leedy does not either expressly or inherently disclose each and every element of independent claim 17, reversal of the 35 U.S.C. §102(b) rejection of independent claim 17 is respectfully requested, as is the allowance of independent claim 17.

Reversal of the 35 U.S.C. §102(b) rejection of claims 18-20 and allowance thereof are respectfully requested as each of these claims depends either directly or indirectly from allowable independent claim 17, among other reasons.

Claim 20 is additionally allowable as Leedy does not expressly or inherently disclose a method that includes forming a support structure by forming a layer of packaging material over the active surface and extending radially outward to at least an outer peripheral edge of the semiconductor substrate. Rather, the frame 18 of Leedy is formed on the backside of a substrate 10 as material is removed from a central location of the backside, while the frame 19 of Leedy is preformed.



B. REJECTIONS UNDER 35 U.S.C. § 103(a)

1. APPLICABLE LAW

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. ADDITIONAL REFERENCE RELIED UPON

*Grigg*

Grigg teaches a process of forming stiffeners through a stereolithographic process on tape 14 for used in Tape Ball Grid Array (TBGA) or Tape Automated Bonding (TAB) applications. Col. 6, lines 5-25; FIG. 2. The stiffeners are formed from a rigid dielectric material, such as a photopolymer, and serve to prevent bending or torsional flexion of the tape 14. Col. 6, lines 23-25; FIG. 2. The stiffeners may also serve to reinforce sprocket or index holes 18 through the tape 14. Col. 6, lines 27-30; FIG. 2.

Grigg teaches that the stiffeners 20 are formed through a stereolithographic process in which the tape 14 is submerged in reservoir of unconsolidated material 86. Col. 13, line 29-32;

FIGS. 11-12. A laser 92 is directed at selected locations on the surface of the tape, the laser energy partially curing the material 86 to form a first layer of the stiffener. Col. 13, lines 54-58. The tape 14 is moved and the laser reactivate to consolidated additional layers of the stiffener 20, as necessary, with the process repeated until the stiffener is fully formed. Col. 13, lines 58-64; FIGS. 11-12.

3. ANALYSIS

a. LEEDY IN VIEW OF GRIGG

Claims 21-34 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over the subject matter taught in Leedy, in view of teachings from Grigg.

Claims 21-34 are allowable as each depends either directly or indirectly from allowable independent claim 17, among other reasons.

It is also respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 21-34 because, without the benefit of hindsight that the claims and disclosure of the '742 Application provide to the Examiner, one of ordinary skill in the art wouldn't have been motivated to combine teachings from Leedy and Grigg in the manner that has been asserted. This is because neither Leedy nor Grigg provides any teaching or suggestion that the stiffening elements of Grigg, which merely reinforce or stiffen parts of a flexible substrate as components are being secured thereto, would be useful in a thinning process. Moreover, in the thinning process of Leedy, it is a thick peripheral portion of a semiconductor

substrate that reinforces the thinned portion of the substrate – no additional element need be formed or on secured to the substrate for reinforcement.

It is further submitted that Leedy and Grigg, taken either together or separately, do not teach or suggest each and every element of several of the rejected claims, as is required to establish a *prima facie* case of obviousness.

Claim 22 is allowable because neither Leedy nor Grigg teaches or suggests a method of forming a support structure that includes forming the outer peripheral portion to include a downwardly extending portion located laterally adjacent to the outer peripheral edge of the semiconductor substrate.

Claim 28 is allowable because neither Leedy nor Grigg teaches or suggests a method of forming a support structure that includes molding a support structure on an active surface of a semiconductor substrate.

Claim 29 is allowable because neither Leedy nor Grigg teaches or suggests a method for thinning a semiconductor substrate that includes securing a semiconductor substrate to a platen with an active surface of the semiconductor substrate facing the platen and a support structure that has been formed on the active surface abutting at least one surface or feature of or one the platen.

It is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 21-34 be reversed, and that each of these claims be allowed.

VIII. CLAIMS APPENDIX

The current status of each claim that has been introduced into the above-referenced application is set forth in CLAIMS APPENDIX to this Appeal Brief.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

XI. CONCLUSION

(A) The subject matter recited in claims 17-20 is novel and, thus, under 35 U.S.C. § 102(b), patentable over the subject matter described in Leedy;

(B) Claims 21-34 are drawn to subject matter that is non-obvious and, thus, under 35 U.S.C. § 103(a), patentable over the subject matter taught in Leedy, in view of teachings from Grigg.

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Therefore, it is respectfully requested that the rejections of claims 17-34 be reversed and that each of these claims be allowed.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Brick G. Power". The signature is fluid and cursive, with the first name "Brick" being more prominent.

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**CLAIMS APPENDIX**

17. A method for thinning a semiconductor substrate, comprising:  
forming a support structure on an active surface of the semiconductor substrate;  
removing material from a back side of the semiconductor substrate to form a thinned  
semiconductor substrate; and  
transporting the thinned semiconductor substrate for further processing.
18. The method of claim 17, wherein forming the support structure comprises forming  
a support ring on the active surface adjacent to an outer peripheral edge of the semiconductor  
substrate.
19. The method of claim 18, wherein forming the support ring comprises forming the  
support ring such that each semiconductor device that has been fabricated on the active surface is  
located within an inner periphery of the support ring and is exposed therethrough.
20. The method of claim 17, wherein forming the support structure includes forming a  
layer of packaging material over the active surface and extending radially outward to at least an  
outer peripheral edge of the semiconductor substrate.
21. The method of claim 17, wherein forming the support structure comprises forming  
the support structure to include an outer peripheral portion that extends beyond an outer  
peripheral edge of the semiconductor substrate.

22. The method of claim 21, wherein forming the support structure further comprises forming the outer peripheral portion to include a downwardly extending portion located laterally adjacent to the outer peripheral edge of the semiconductor substrate.

23. The method of claim 17, wherein forming the support structure comprises:  
forming a layer comprising unconsolidated material over at least an outer peripheral portion of the active surface; and  
at least partially consolidating the unconsolidated material within at least outer peripheral regions of the layer.

24. The method of claim 23, wherein at least partially consolidated the unconsolidated material comprises directing a focused energy beam onto at least the outer peripheral regions of the layer.

25. The method of claim 24, wherein directing the focused energy beam comprises directing a laser beam onto at least the outer peripheral regions of the layer.

26. The method of claim 17, wherein forming the support structure comprises stereolithographically forming the support structure.

27. The method of claim 17, wherein forming the support structure comprises:  
positioning a preformed film of support material over the active surface; and  
removing selected regions of the preformed film.

28. The method of claim 17, wherein forming the support structure comprises  
molding the support structure on the active surface.

29. The method of claim 17, further comprising:  
securing the semiconductor substrate to a platen with the active surface facing the platen and the  
support structure abutting at least one surface or feature of or on the platen.

30. The method of claim 29, wherein securing the semiconductor substrate comprises  
applying a negative pressure to the active surface.

31. The method of claim 29, wherein securing the semiconductor substrate includes  
sealing the support structure against the at least one surface or feature.

32. The method of claim 17, wherein removing material from the back side of the  
semiconductor substrate comprises at least one of chemically and mechanically removing  
material from the back side.



33. The method of claim 17, wherein removing material from the back side of the semiconductor substrate comprises back grinding.

34. The method of claim 17, wherein the support structure supports the thinned semiconductor substrate during transporting thereof.